International Journal Of Engineering Research & Management Technology

ISSN: 2348-4039

Email: editor@ijermt.org May- 2014 Volume 1, Issue 3 Website: ijermt.org

A Modified Buck Converter With Improved Performance For The Mitigation Of Power Quality Issues

C.Jeeva
M.Tech (EEE) student

D.V.Avasthi
EEE Department

Subharti Institute of Technology & Engineering
SVSU., Meerut

ABSTRACT

The buck converter is a dc voltage step down or current step up converter with high power efficiency and potential for use in low voltage applications. The major limitation of buck converter circuit lies in the semiconductor switch causing switching power loss, harmonic voltages, harmonic currents, reactive power and low power factor on ac side. The main objective of this work, therefore, is to abridge these limitations through improved design so that the switching power loss, harmonic components of current and voltage and reactive power in the buck converter circuit can be minimized and power factor of the buck converter circuit can be brought as near to unity as possible in order that power loss is minimum and power efficiency of the converter is improved.

Indexing terms: Power factor, Buck converter, Boost converter, Dual Boost converter, Voltage mode control, Average Current mode control.

PFC buck converters form the key area of research due to industries focus on power quality, energy conservation and energy efficiency. Converters providing stable DC output voltage with high input power factor are in great demand in the power electronics industry. These are an ideal choice for offline power supply and other important AC–DC power conversion applications matching the need of power quality terms and standards.

The circuit diagram of a buck converter using power BJT is shown below in figure (1). It can preferably be replaced by the Power MosFET or some other fast switching device with low switching loss. The circuit operates like a step-down converter in which Va< Vs. The operation of Buck Converter can be described in two modes. Mode-1 begins when transistor Q1 is switched ON at t=0 and the input current rises, flows through filter inductor L, filter capacitor C and load resistor R. Mode-2 begins when transistor Q1 is switched OFF at $t=t_1$. The freewheeling diode D_m conducts because of the energy stored in the inductor and the current flow through L, C, load and diode Dm.

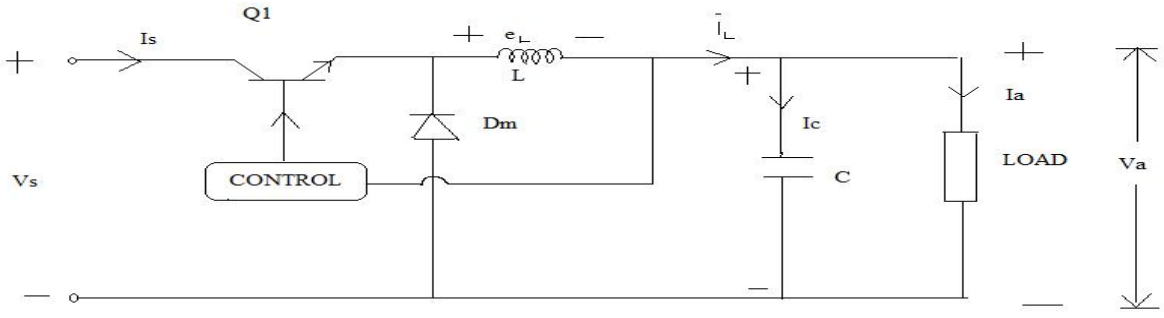

Fig 1. Circuit Diagram of Buck Converter

Current from the line in the circuit of Fig. 1 is drawn only when the input voltage is greater than the output voltage i.e., Vs > Va. As a consequence, notches appear in the line current around zero crossing of the line voltage, causing distortion. Various drawbacks such as switching power loss, harmonic voltages, harmonic currents, reactive power and low power factor on ac side are observed in the buck converter circuit which makes its operation disadvantageous for practical applications.

Power factor correction of the buck converter is the important step to rid most of the practical problems described above. PFC will automatically cause reactive power to disappear and reduce harmonics by making AC voltages and currents almost in phase.

Harmonic Distortion and PF:

Assuming an ideal sinusoidal input voltage source, total rms current = I_{rms} and power factor = cosΦ; but when the current waveform is not an ideal sinusoid, then power factor can be expressed as the product of the distortion factor and the displacement factor. The distortion factor K_d is the ratio of the fundamental root mean- square (RMS) current (Irms)) to the total RMS current (I_{rms1}).

$K_d = I_{rms1} / I_{rms}$

$I_{rms1} = K_d I_{rms}$

The displacement factor K_θ is the cosine of the displacement angle (φ) between the fundamental input current and the input voltage. $K_\theta = \cos \varphi$.

For sinusoidal voltage and non-sinusoidal current, the equation can be expressed as:

$$PF = \frac{V_{rms} I_{1,rms} \cos\varnothing}{V_{rms} \times I_{rms}} = \frac{I_{1,rms}}{I_{rms}} \cos\varnothing = K_d \cos\varnothing$$

$$PF = K_d K_\theta$$

In this case, the power factor depends on both harmonic content and displacement factor. The displacement factor K_θ can be made unity with a capacitor or inductor, but making the distortion factor K_d unity is more difficult. In addition, the harmonic currents generated by the converter in the power source affects other equipment. From the power factor triangle in Fig (2) it is seen that by reducing the distortion angle Θ i.e., by reducing current harmonics we can improve power factor.

The total harmonic distortion (THD) is given by

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1}$$

Where V_n is nth harmonic amplitude and V_1 is fundamental Fig.3: Harmonic distortion and Power factor triangle

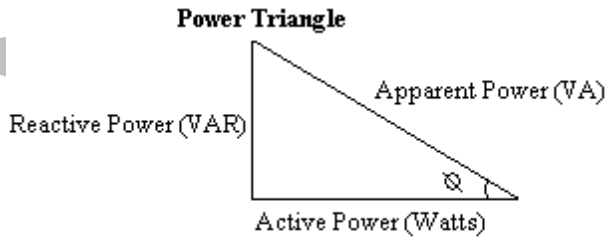

Fig.2: Harmonic distortion and Power factor triangle

The two major power factor correction techniques are Active PFC (APFC) and Passive PFC(PPFC) technique. A passive PFC rarely achieves low Total Harmonic Distortion (THD). Also, the passive elements are normally bulky and heavy.

The Active Power Factor Correction (APFC) is a method to improve the power factor near to unity, reduces harmonics distortion noticeably and automatically corrects the distorted line current. It offers better THD and is significantly smaller and lighter than a passive PFC circuit. The active methods of PFC, which involve the shaping of the line current, using switching devices such as MOSFETs and IGBTs, is a result of advances in power semiconductor devices.

Figure 3 suggests the proposed improved buck convertor topology. The improvement is accomplished by the addition two of diodes and a semiconductor power switch. The modified buck converter is operated in the critical continuous conduction mode (CRM) by applying constant on time control (COT). The two diodes and semiconductor power switch are added in the PFC converter operated with PWM. The voltage across the main switch of the buck converter is almost clamped to the input voltage and higher efficiency of the converter is achieved within the universal input voltage range. The switching power loss in the buck converter occurs due to the dead zones causing deterioration in the performance. The operation of the buck converter in critical continuous conduction mode eliminates these which reduces reverse recovery loss in the diodes and accomplishes zero voltage switching (ZVS) of the switching device.

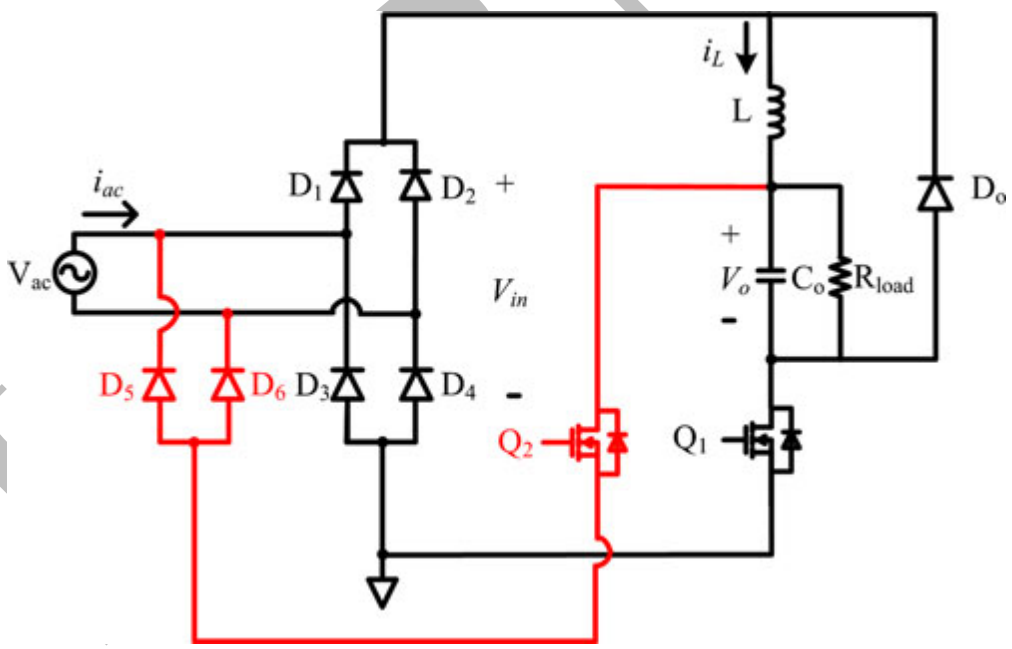

Fig. 3. Improved buck PFC converter.

The operation of the proposed modified converter in CRM mode can be understood from figures 4(a) to (d) which are self explanatory and can be referred to in the literature. To make the analysis simpler the transitions between the switches and the output diode D_o are omitted. After that, there still exist eight operational stages in a line

period the equivalent circuits for which have been shown in Fig (4) with components shown in the dark lines representing circuit part in operation.

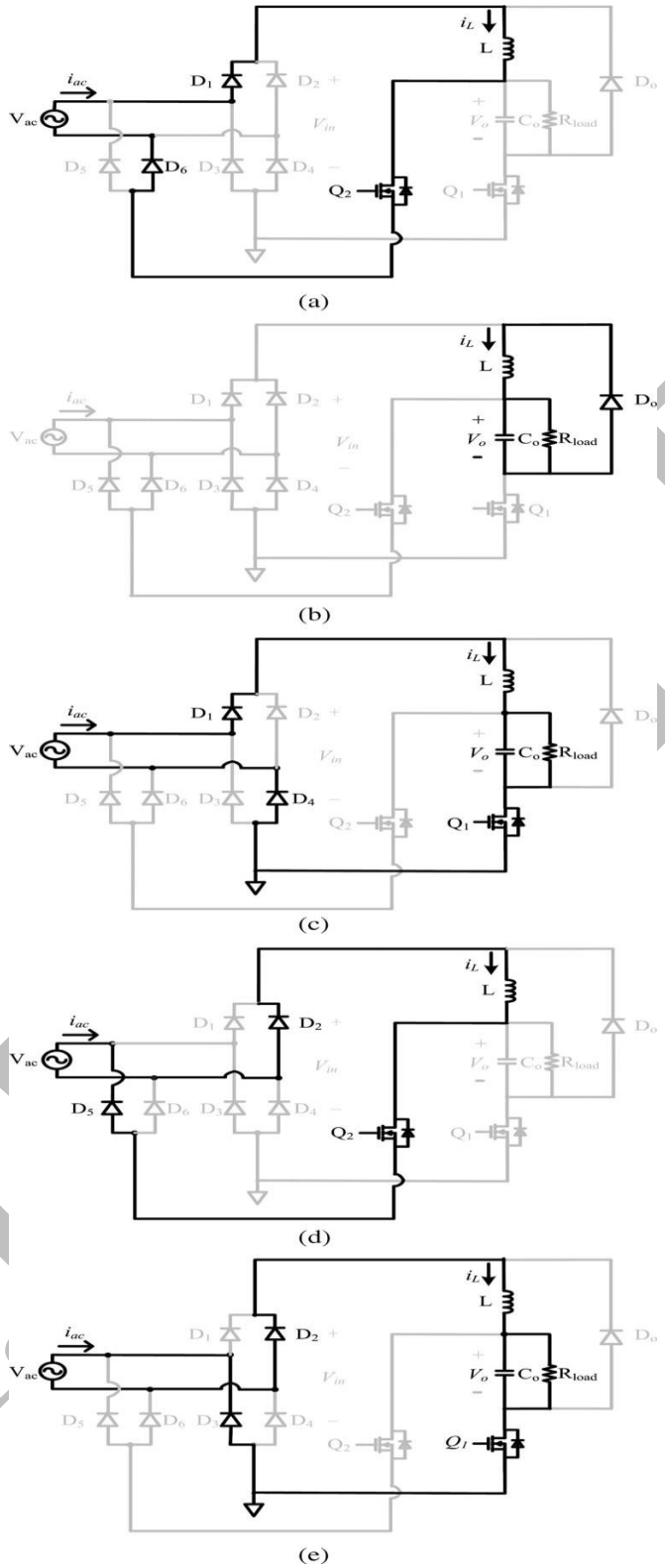

Figure (4). Equivalent circuits of the proposed converter in eight stages.

An improved COT control is applied for the proposed buck PFC converter to force it that operates in CRM, as shown in Fig. 5. The output voltage is detected with a level-shift circuit formed by a high-voltage transistor Q2 and the resistors Ra1~Ra4. Some key waveforms are shown in Fig 6.

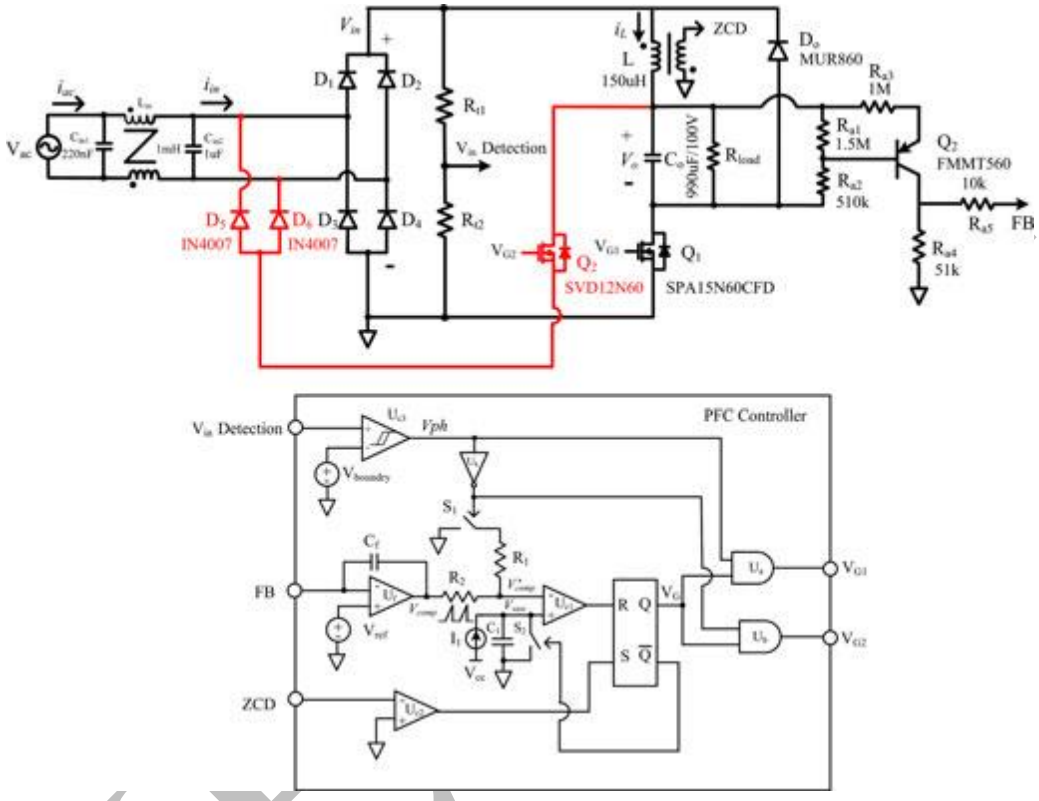

Fig. 5. Schematic of the proposed buck PFC converter with an improved COT control.

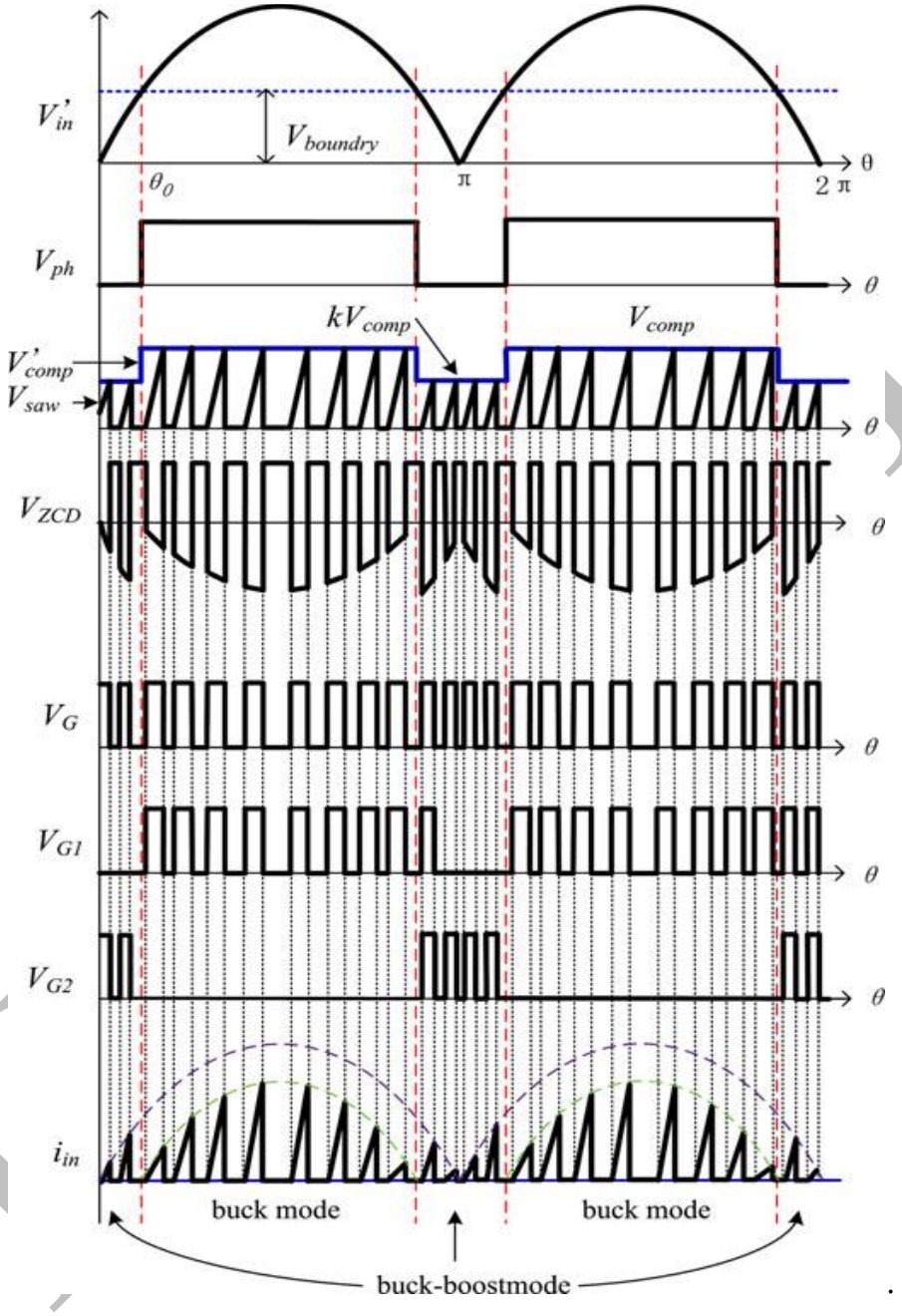

Fig. 6. Key waveforms of rms in the improved COT control diagram.

As shown in Fig. 3, the control signal V_{ph} used to control the converter either in buck mode or buck-boost mode is achieved by comparing the detected V_{in} signal V'_{in} with a voltage reference $V_{boundry}$. Usually, $V_{boundry}$ is set to reflect the output voltage V_o with the same ratio as that V'_{in} reflects V_{in} . V_{ph} is high logic when V'_{in} is higher than $V_{boundry}$ and is low logic when V'_{in} is lower than $V_{boundry}$. The detected output signal V_{FB} is sent to the negative input of the error amplifier U_f . The error between V_{FB} and the set reference V_{ref} is amplified by the compensation networks C_f and an amplified error signal V_{comp} is achieved. The dc voltage signal V_{comp} applied to control the conduction period T_{ON} is achieved from V_{comp} through a control networks formed by resistors R_1 and R_2 and switch S_1 . Switch S_1 is controlled by the control signal V_{ph}. The proposed converter operates in buck mode when S_1 is OFF and operates in buck boost mode when S_1 is ON. V_{comp} is a step function controlled by V_{ph}, as shown in (1)

$$V_{comp} = \{Vcomp \quad Vin > Vo$$

$$\{k \cdot Vcomp \quad Vin \leq Vo \quad (1)$$

Where k is a coefficient equal to R1 /(R_1+R_2)

Similar to the conventional COT control, a constant current source I_1 , capacitor
C_1 , and switch S_2 are used to generate a saw tooth waveform V_{saw}. When V_{saw} reaches $V_{comp,}$ the output of comparator U_{c1} jumps from low level to high level. This level transition resets the driving signal from high level to low level.
The zero-crossing point of the inductor current i_L is detected by the auxiliary winding of the inductor L. This inductor current zero-crossing detection signal V_{ZCD} can be applied in both buck and buck-boost modes. When the inductor current i_L falls to zero, the output voltage auxiliary winding V_{ZCD} starts to fall. Once V_{ZCD} falls to zero, the output of comparator U_{c2} jumps from low level to high level. This level transition sets the driving signal from low level to high level.
According to the aforementioned analysis, the rising slope of V_{saw} is constant due to the constant current source I_1 charging during the whole line period. Therefore, the ON-time (T_{ON}) of the switches is determined by V'_{comp} proportionally. Smaller value of k leads to smaller T_{ON} and smaller peak values of i_L when the proposed converter is operating in buck-boost mode. As shown in Figs. 3 and 4, the driving signals V_{G1} and V_{G2} are controlled by V_{ph} for the different operation modes alternately. Different coefficient k results in the different PF correction performance and the overall efficiency which has to be optimized.

CONCLUSION

The improved buck PFC converter topology proposed in this paper is easy to fabricate as the structure of the topology is simple. To operate in CRM, an improved COT control is proposed. Near unity PF can be accomplished and the input current harmonics can meet the IEC61000-3-2 class C standard within the universal input voltage range, whereas the efficiency is not deteriorated compared to the conventional buck converter. The main disadvantage observed in the proposed topology is that two diodes and a switch are required and the added switch needs a floating driving circuit. However, the cost and size increase is nominal compared to the whole cost and size. The Matlab Simulink model for the proposed model is presented and the waveforms at each stage are presented. On the whole, the proposed converter is very suitable for industrial applications.

REFERENCES

1. Improved buck PFC converter Development of Power Factor Controller using PIC Microcontroller Pankaj Trivedi 1, Tejbir Singh 2, and D. V. Avasthi; International Journal of Emerging trends in Engineering and Development Issue 2, Vol.6 (September 2012)
2. Xiaogao Xie, Member, IEEE, Chen Zhao, Member, IEEE, Lingwei Zheng, Member, IEEE, and Shirong Liu IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 28, NO. 5, MAY 2013
3. Y. Fei, R. Xinbo, Y. Yang, and Y. Zhihong, "Interleaved critical current mode boost PFC converter with coupled inductor," IEEE Trans. Power Electron., vol. 26, no. 9, pp. 2404–2413, Sep. 2011.
4. E. L. Huber, B. T. Irving, and M. M. Jovanovich, "Effect of valley switching and switching-frequency limitation on line-current Distortions of DCM/CCM boundary boost PFC converters," IEEE Trans. Power Electron., vol. 24, no. 2, pp. 339–347, Feb. 2009.